

Form PTO-1449

U.S. DEPARTMENT OF COMMERCE  
PATENT AND TRADEMARK OFFICEATTY. DOCKET NO.  
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U.S. PATENT  
678/118/99  
157/118/99

## U.S. PATENT DOCUMENTS

*Examiner Initial		Document Number	Date	Name	Class	Subclass	Filing Date If Appropriate
WDR	AA	5,253,255	10/12/93	Carbine			
	AB	5,404,526	4/4/95	Dosch et al.			
	AC	5,406,497	04/11/95	Alzheimer et al.			
	AD	5,550,839	08/27/96	Buch et al.			
	AE	5,684,808	11/04/97	Valind			
	AF	5,689,517	11/18/97	Ruparel			
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	AH	5,812,561	09/22/98	Giles et al.			
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	AJ	5,831,993	11/3/98	Graef			
WDR	AK	5,862,149	01/19/99	Carpenter et al.			

## FOREIGN PATENT DOCUMENTS

		Document Number	Date	Country	Class	Subclass	Translation	
							Yes	No
	AL							
	AM							
	AN							
	AO							
	AP							

## OTHER REFERENCES (including Author, Title, Date, Pertinent Pages, Etc.)

WDR	AR	WDR	Ghosh et al. "A Design-for-Testability Technique for Register-Transfer Level Circuits Using Control/Data Flow Extraction", IEEE Transactions on Computer Aided Design of Integrated Circuits and Systems, August 1998, pp. 706-723.
WDR	AS	WDR	Lin et al. "Cost-Free Scan: A Low-Overhead Scan Path Design", IEEE Transactions on Computer Aided Design of Integrated Circuits and Systems, September 1998, pp. 852-861.
WDR	AT	WDR	Lin et al. "Test-Point Insertion: Scan Paths Through Functional Logic", IEEE Transactions on Computer Aided Design of Integrated Circuits and Systems, September 1998, pp. 838-851.

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*Examiner Initial		Document Number	Date	Name	Class	Subclass	Filing Date If Appropriate
um	AA	5,909,453	06/01/99	Kelem et al.			
um	AB	5,920,575	07/06/99	Gregor et al.			
	AC						
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um	AR		Runyon, Stan, "Testing Big Chips", IEEE Spectrum, April 1999, pp. 49-55.
	AS		
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